//testbench

module testbench;

reg D= 0, clk = 0;

wire Q;

flipflop uut(D, clk, Q);

always begin

clk = ~clk;

#10;

end

initial begin

$dumpfile("flipflop.vcd");

$dumpvars(0,testbench);

D=1; #40;

D=0; #40;

$finish;

end

endmodule

//actual design

module flipflop(D, clk, Q);

input D, clk;

output reg Q;

always@(posedge clk)

begin

Q=D;

end

endmodule